Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70010

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2025
Third Semester
VLSI Design
P23VD311 - ASIC DESIGN
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	How is logical effort used in digital design?	2	K2	CO1
2.	List the different technologies used in IC.	2	K2	CO1
3.	In what ways is a metal antifuse superior to a poly diffusion antifuse?	2	K2	CO2
4.	How does static RAM differ from dynamic RAM?	2	K2	CO2
5.	List the key features of the Altera FLEX FPGA family.	2	K2	CO3
6.	Define schematic entry.	2	K2	CO3
7.	Compare VHDL and Verilog in terms of syntax and usage.	2	K2	CO4
8.	Describe the purpose of functional simulation in circuit design.	2	K2	CO4
9.	Mention some objectives of system partitioning.	2	K2	CO5
10.	Name two common methods used for partitioning in circuit design.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Identify the sources of parasitic capacitance in MOS transistors and their effects on circuits.	13	K2	CO1

(OR)

	b)	Construct the data path logic of a 6-bit array multiplier using a different data path.	13	K2	CO1
12.	a)	With a block diagram, explain the architecture of the ALTERA flex cell.	13	K4	CO2
		(OR)			
	b)	Discuss the various termination schemes used in programmable ASIC I/O cells.	13	K4	CO2
13.	a)	Discuss the various PLA tools for logic minimization in ASIC's.	13	K4	CO3
		(OR)			
	b)	Describe the interconnect architecture used in an Actel ACT.	13	K4	CO3
14.	a)	Compare and contrast gate-level simulation and structural simulation in VHDL modelling.	13	K2	CO4
		(OR)			
	b)	Describe the architecture and operation of boundary scan as applied to ASIC design.	13	K2	CO4
15.	a)	How does placement impact timing, power and routability in the physical design flow?	13	K3	CO5
		(OR)			
	b)	Describe the global routing process between blocks in ASIC design.	13	K3	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Compare Actel ACT, Xilinx LCA, and Altera FLEX/MAX FPGA families focusing on architecture, configuration, and reliability.	15	K4	CO3
		(OR)			
	b)	Assess how fault simulation enhances test coverage and reliability during pre-manufacturing verification of ASICs	15	K2	CO4